A METHOD AND APPARATUS FOR ADDRESSING IN MASS STORAGE NON-VOLATILE MEMORY DEVICES

BACKGROUND OF THE INVENTION

[001] Memory devices for non-volatile storage of information are currently in widespread use today in numerous applications. For example, flash memory devices, such as, for example MultiMediaCard (MMC) and Secure Digital (SD) card may be used with cellular telephones, personal digital assistants, digital cameras and music players.

[002] Access operations to data within a flash memory device, such as SD and MMC are performed via read/write commands. A portion of the command is a specific address representing the location of a specific data within the memory device. Currently, addresses are expressed as byte addressed 32-bit arguments. The use of a 32-bit argument may produce 2^{31} different byte addresses, which may individualize up to 4GBytes of data. There is a need for another solution for addressing in mass storage memory devices having a larger capacity.

BRIEF DESCRIPTION OF THE DRAWINGS

[003]   The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanied drawings in which:

[004]   Fig. 1 is a block-diagram illustration of a host command according to some embodiments of the present invention;

[005]   Fig. 2 is a block-diagram illustration of a host device helpful in understanding the dual-mode addressing arrangement according to some embodiments of the present invention;

[006]   Fig. 3 is a block-diagram illustration of a host device helpful in understanding the dual-mode addressing arrangement according to some embodiments of the present invention; and

[007]   Fig. 4 is flowchart diagram illustration of a portion of a read operation or a write operation according to some embodiments of the present invention.

[008]   It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF THE INVENTION

[009] Existing mass storage memory devices currently may have the capacity of storing up to 1GB, and therefore byte addressing is suitable and is used in existing mass storage memory devices. The use of byte addressing is not suitable for new mass storage memory devices having a larger capacity.

[0010] A mode of addressing suitable for large capacity mass storage memory devices having more than 2GB storage space may be block addressing. The address argument, in this case, represents an address of the first byte of a specific block. A block may comprise a predefined number of bytes, such as, for example, 512 bytes, 2048 bytes or 8192 bytes. A simple block addressing system, however, would be backwards incompatible with byte addressing standards.

[0011] In accordance with embodiments of the present invention, there is presented a hybrid memory addressing system. The use of the existing byte addressing mode to perform read and write operations by an existing host on a new memory device (having a capacity larger than 2GB) may enable access only to the first 2GB of the memory space on the new memory device. The use of block addressing mode to perform read and write operations on a new memory device (having a capacity larger than 2GB) may not be backwards compatible and may not enable to perform read and write operations on a byte-addressing memory device.

[0012] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

[0013] Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing," "computing," "calculating," "determining," or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the

computing system's memories, registers or other such information storage, transmission or display devices.

[0014] Embodiments of the present invention may include apparatus for performing the operation herein. This apparatus may be specially constructed for the desired purposes, or it may comprise a general-purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but not limited to, any type of disk, including floppy disks, optical disks, magnetic-optical disks, read-only memories (ROM's), compact disc read-only memories (CD-ROM's), random access memories (RAM's), electrically programmable read-only memories (EPROM's), electrically erasable and programmable read only memories (EEPROM's), FLASH memory, magnetic or optical cards, or any other type of media suitable for storing electronic instructions and capable of being coupled to a computer system.

[0015] The processes and displays presented herein are not inherently related to any particular apparatus. Various general-purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct a more specialized apparatus to perform the desired method. The desired structure for a variety of these systems will appear from the description below. In addition, embodiments of the present invention are not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of embodiments of the invention as described herein.

[0016] It should be appreciated that according to some embodiments of the present invention, the method described below, may be implemented in machine-executable instructions. These instructions may be used to cause a general-purpose or special-purpose processor that is programmed with the instructions to perform the operations described. Alternatively, the operations may be performed by specific hardware that may contain hardwired logic for performing the operations, or by any combination of programmed computer components and custom hardware components.

[0017] The method may be provided as a computer program product that may include a machine-readable medium having stored thereon instructions that may be used to

program a computer (or other electronic devices) to perform the method. For the purposes of this specification, the terms "machine-readable medium" may include any medium that is capable of storing or encoding a sequence of instructions for execution by the machine and that cause the machine to perform any one of the methodologies of the present invention. The term "machine-readable medium may accordingly include, but not limited to, solid-state memories, optical and magnetic disks, and a carrier wave that encodes a data signal.

[0018] In some embodiments of the present invention, a mass storage media device is used. In the exemplary embodiments below, the architecture of a MultiMediaCard (MMC) or Secure Digital (SD) card is used. However, it should be understood to a person skilled in the art that the invention is not limited to MMC and SD cards only and may be equally applicable to other memory devices, such as for example, compact flash cards, memory stick, XD cards, disk on key and IBM Microdrive.

[0019] Although the scope of the present invention is not limited in this respect, the system and method disclosed herein may be implemented in many wired or wireless, handheld, and portable communication and entertainment devices. By way of example, communication and entertainment devices may include wireless and cellular telephones, smart telephones, personal digital assistants (PDAs), digital cameras, digital music players, and video games consoles. Alternatively, according to other embodiments of the present invention, the system and method disclosed herein may be implemented in computers.

[0020] Some embodiments of the present invention are directed to a method and apparatus to access data stored on mass storage memory devices having byte or block addressing with a single command structure capable of having instructions for both a byte addressing mode and a block addressing mode. The usage of an existing un-used physical bit of a byte addressing command may enable backwards compatibility to existing mass storage data memory devices and enable to interpret the address argument according to the appropriate addressing mode.

[0021] Reference is now made to Fig. 1, which is a simplified block-diagram illustration of a host command according to some embodiments of the present invention. In the exemplary illustration described below, a host command 10 may comprise 48 bits. One of ordinary skill in the art will understand that the selection of

the command size and the functional division within the command is for illustration purposes only and embodiments of the present invention are not restricted to such a configuration.

[0022] Block 12 represents bit 0, which may be the "Start bit", block 14 represents bit 1, which may be the "Transmission bit" and block 16 represents bits 2 to 7 which may comprise the command code. Block 20 represents bits 40 to 46 and may contain an error detection code and block 22 represents bit 47, which may be the "End bit".

[0023] In the exemplary 48-bit host command 10, block 18 represents bits 8 to 39, which may comprise a 32-bit address argument. Block 18 may be divided into two portions. The first portion, block 18A, which in this exemplary embodiment represents bit 8, may function as an addressing mode field as explained in detail hereinbelow in Figs. 2 and 3. The second portion, block 18B, which in this exemplary embodiment represents bits 9 to 39, may represent a 31-bit address argument.

[0024] It will be understood by a person skilled in the art that a 32-bit address argument is merely one exemplary embodiment, for example, compatible with the MMC and SD protocols, and embodiments of the present invention are not limited in this respect. According to other embodiments of the present invention, an address argument may comprise more or less than 32 bits, at least one of the bits may be an unused bit.

[0025] Writing data onto a mass storage device and reading the data from the mass storage memory device may be executed by sending write and read commands from the host device to a specific location on the memory device. The address argument represents an address within the address space of the mass storage memory device. Currently, to access mass storage data memory devices, such as, for example, MMC and SD, the address argument represents an address of a specific byte, namely the mode of addressing is byte addressing.

[0026] Theoretically, a 32-bit address argument may individualize up to 4 gigabytes (GB) of data. However, according to the protocols related to existing mass storage memory devices, such as MMC and SD, the least significant bit (LSB) or the most significant bit (MSB), namely bit 0 or bit 31 of the address argument is always 0. Therefore, the remaining 31 bits may individualize up to 2GB.

[0027] Reference is now made to Fig. 2 and Fig. 3, which are block-diagram illustrations of a host device helpful in understanding the dual-mode addressing arrangement according to some embodiments of the present invention.

[0028] As shown in Fig. 2, a host device 30 may comprise a memory unit 32 having a byte-addressing system suitable for byte-addressing and a controller 36 to send commands to memory unit 32. Controller 36 may store a command having an address portion 40. An addressing mode field 42 may store the value zero to indicate that the address argument 44 is a byte addressing argument. Therefore, the command associated with address argument 44 may access data stored within memory unit 32 using byte addressing mode.

[0029] As shown in Fig. 3, host device 30 may comprise a memory unit 38 having a block-addressing system suitable for block addressing. Controller 36 may store a command having an address portion 56. An addressing mode field 58 may store the value one to indicate that the address argument 60 is a block addressing argument. Therefore, the command associated with address argument 60 may access data stored within memory unit 32 using block-addressing mode

[0030] According to some embodiments of the present invention, a single memory device may be compatible with both byte-addressing and block-addressing systems. It will be understood to a person skilled in the art that an application may switch between byte addressing and block addressing modes as applicable.

[0031] In order to communicate to the host which addressing system is intended by the argument, the unused LSB or MSB, for example the 9th bit (bit 8) of host command 10 may be used as an addressing mode field. Thus, for example, if the 9th bit of command 10 equals zero (as illustrated in Fig. 2), then the remaining 31 bits, (bits 9 to 39) may represent a byte address. If the 9th bit of command 10 equals one (as illustrated in Fig. 3), then the remaining 31 bits, (bits 9 to 39) may represent a block address. It will be understood that in accordance with embodiments of the present invention, Figs. 2 and 3 may refer to the same memory device compatible with both addressing systems.

[0032] It should be understood by a person skill in the art that the addressing mode field may be used for other purposes in the system such as, for example, management of program execution, data process and card wear leveling management

[0033] Reference is additionally made to Fig. 4, which is flowchart diagram illustration of a portion of a read operation or a write operation according to some embodiments of the present invention.

[0034] At operation 400, controller 36 of device 30 may be notified of a read or write command. Controller 36 then may determine whether the Addressing Mode field (which may be the least significant bit (LSB) or the most significant bit (MSB) of the address argument within the received command) has the value of zero. (operation 410). If the value of the Addressing Mode field is zero, controller 36 may refer to the address argument as a byte-addressing argument 44 (operation 420). The controller 36 then may enable access to a specific byte address within the byte addressing space 34 based on the data within the address argument (operation 430). If the value of the Addressing Mode field is one, controller 36 may refer to the address argument 18B as a block-addressing argument 60 (operation 440). The controller 36 then may enable access to the first byte of a specific block address within the block addressing space 44 based on the data within the address argument (operation 450).

[0035] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those of ordinary skill in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.